

**REMARKS**

The Final Office Action mailed November 19, 2003, has been received and reviewed. Claims 1 through 46 are currently pending in the application. Claims 2, 9, 17 through 23, 25, 32, and 40 through 46 have been withdrawn from consideration as being drawn to non-elected invention(s). Claims 1, 3 through 8, 10 through 16, 24, 26 through 31, and 33 through 39 stand rejected.

Per this response, Applicant has cancelled claims 2, 3, 5, 14 through 19, 25, 26, 28, 34, and 37 through 42, amended claims 1, 4, 6 through 13, 24, 27, 29 through 32, 36 and 43, and respectfully requests reconsideration of the application as proposed amended herein.

**Information Disclosure Statement(s)**

Applicant notes the filing of Information Disclosure Statements herein on June 2, 2003, September 29, 2003, and on or about November 13, 2003, and notes that no copies of the PTO-1449s or PTO/SB/08s were returned with the outstanding Office Action. Applicant respectfully requests that the information cited on the PTO-1449s and PTO/SB/08s be made of record herein.

**35 U.S.C. § 102(b) Anticipation Rejections**

**Anticipation Rejection Based on Japanese Patent No. JP 07-302860 A to Mura**

Claims 1, 3 through 5, 8, 10 through 14, 24, 26 through 28, 31, and 33 through 37 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Mura (Japanese Patent No. JP 07-302860 A). Applicant respectfully traverses this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claims 1, 4, 8 and 10 through 13

Independent claim 1, as amended herein, is directed to a method for aligning a semiconductor device package with a carrier substrate for electrical interconnection therebetween. The method comprises: forming at least two channels through the semiconductor device package from a first major surface thereof to a second, opposing major surface thereof; providing a major surface of the carrier substrate with at least two alignment features including forming at least two holes in the carrier substrate, each of which are spaced and positioned in respective correspondence to the at least two channels; placing the semiconductor device package over the carrier substrate with the first major surface of the semiconductor package facing the major surface of the carrier substrate; aligning the at least two channels formed in the semiconductor device package with the at least two alignment features of the carrier substrate; *providing at least two pins, wherein at least one of the at least two pins includes a mechanical self-locking mechanism proximate at least one end thereof*; placing the at least two pins through the at least two channels and into the at least two holes; and *engaging a portion of at least one of the second major surface of the semiconductor device package and a second, opposing surface of the carrier surface with the mechanical self-locking mechanism.*

The Examiner cites Mura as disclosing a method which comprises: forming at least two channels (11a) through a semiconductor device package (1) from a first major surface thereof to a second, opposing major surface thereof; providing a major surface of a carrier substrate (2) with at least two alignment features (22) spaced and positioned in respective correspondence to the at least two channels; placing the semiconductor device package over the carrier substrate and aligning the at least two channels with the at least two alignment features. However, Applicant submits that Mura fails to teach all of the limitations of claim 1 of the presently claimed invention.

Applicant notes that, while Mura discloses the use of an alignment pin to align a semiconductor device package and a substrate, that Mura fails to disclose providing at least two pins *wherein at least one of the at least two pins includes a mechanical self-locking mechanism*

*proximate at least one end thereof.* It is further noted that, while such subject matter was generally included in the present application in the form of a dependent claim (e.g., claim 10), the Examiner did not cite any explicit teaching by Mura regarding such subject matter. Additionally, Mura fails to teach engaging a portion of at least one of the second major surface of the semiconductor device package and a second, opposing surface of the carrier substrate with the mechanical self locking mechanism.

Applicant, therefore, submits that claim 1 is clearly not anticipated by Mura. Applicant further submits that claims 4, 8 and 10 through 13 are allowable as being dependent from an allowable base claim as well as for the additional patentable subject matter introduced thereby.

With respect to claim 8, Applicant submits that Mura fails to teach affixing the at least two pins to both the semiconductor device package and to the carrier substrate. Rather, Mura teaches that one end of the alignment pin is press fit into a corresponding hole in the semiconductor device package while the other end is free to float within a corresponding hole in the substrate. Such relative movement between the alignment pin and the substrate is desired so that a shoulder of the pin may act as a stop between the semiconductor device package and the substrate to prevent undesirable squashing of the solder balls during reflow thereof. (See, e.g., Mura, paragraph [0022]).

With respect to claim 10, Applicant submits that Mura fails to teach forming a mechanical self-locking mechanism at a first end and at a second end of the at least one pin.

With respect to claim 11, Applicant submits that Mura fails to teach removing the at least two pins subsequent to the alignment of the at least two channels with the at least two alignment features. Nor does the Examiner point to any specific teaching by Mura of such subject matter.

With respect to claims 12 and 13, Applicant submits that Mura fails to teach that placing the semiconductor device package over the carrier substrate is effected using a pick and place device.

With respect to claim 13, Applicant submits that Mura fails to teach that the pick and place device is used to align the semiconductor device package with the carrier substrate by

carrying the at least two pins with the head of the pick and place device and inserting the at least two pins through the at least two channels and the at least two holes.

Applicant, therefore, respectfully requests reconsideration and allowance of claims 1, 4, 8 and 10 through 13.

Claims 24, 27, 31, 33, 35 and 36

Independent claim 24, as amended herein, is directed to a method of testing a semiconductor device package having a plurality of discrete conductive elements disposed in a pattern on a surface thereof. The method comprises: providing a carrier substrate having a plurality of terminal pads arranged in a pattern corresponding to a mirror image of the pattern of discrete conductive elements; forming at least two channels in the semiconductor device package, each channel passing from a first surface thereof to a second, opposing surface thereof; providing the carrier substrate with at least two alignment features including forming at least two holes in the carrier substrate, each of which are respectively spaced and positioned in correspondence to one of the at least two channels; placing the semiconductor device package over the carrier substrate; aligning each channel of the at least two channels formed in the semiconductor device package with a corresponding alignment feature of the at least two alignment features of the carrier substrate including placing pins through the at least two channels and into the at least two holes; electrically contacting each discrete conductive element of the plurality with a terminal pad of the plurality; passing at least one electrical signal between the semiconductor device package and the carrier substrate; and *removing the pins subsequent to the alignment of each of the at least two channels with a corresponding alignment feature of the at least two alignment features.*

The Examiner cites Mura as disclosing a method which comprises: forming at least two channels (11a) through a semiconductor device package (1) from a first major surface thereof to a second, opposing major surface thereof; providing a major surface of a carrier substrate (2) with at least two alignment features (22) spaced and positioned in respective correspondence to the at least two channels; placing the semiconductor device package over the carrier substrate and

aligning the at least two channels with the at least two alignment features. However, Applicant submits that Mura fails to teach all of the limitations of claim 1 of the presently claimed invention. However, Applicant submits that Mura fails to teach all of the limitations of claim 24 of the presently claimed invention.

Applicant notes that, while Mura discloses the use of an alignment pin to align a semiconductor device package and a substrate, that Mura fails to disclose *removing the pins subsequent to the alignment of each of the at least two channels with a corresponding alignment feature of the at least two alignment features*. Indeed, Mura teaches that the alignment pins are to remain between the semiconductor device package and the substrate during reflow of the solder balls thereby essentially capturing the alignment pins between the two components.

Applicant, therefore, submits that claim 24 is clearly not anticipated by Mura. Applicant further submits that claims 27, 31, 33, 35 and 36 are allowable as being dependent from an allowable base claim as well as for the additional patentable subject matter introduced thereby.

With respect to claim 31, Applicant submits that Mura fails to teach affixing the at least two pins to both the semiconductor device package and to the carrier substrate. Rather, Mura teaches that one end of the alignment pin is press fit into a corresponding hole in the semiconductor device package while the other end is free to float within a corresponding hole in the substrate. Such relative movement between the alignment pin and the substrate is desired so that a shoulder of the pin may act as a stop between the semiconductor device package and the substrate to prevent undesirable squashing of the solder balls during reflow thereof. (See, e.g., Mura, paragraph [0022]).

With respect to claim 33, Applicant submits that Mura fails to teach forming a mechanical self-locking mechanism proximate at least one end of each pin.

With respect to claims 35 and 36, Applicant submits that Mura fails to teach that placing the semiconductor device package over the carrier substrate is effected using a pick and place device.

With respect to claim 36, Applicant submits that Mura fails to teach that the pick and place device is used to align the semiconductor device package with the carrier substrate by

carrying the at least two pins with the head of the pick and place device and inserting the at least two pins through the at least two channels and the at least two holes.

Applicant, therefore, respectfully requests reconsideration and allowance of claims 1, 4, 8 and 10 through 13.

### **35 U.S.C. § 103(a) Obviousness Rejections**

#### Obviousness Rejection Based on Japanese Patent No. JP 07-302860 A to Mura in View of U.S. Patent No. 5,350,713 to Liang

Claims 6, 7, 15, 16, 29, 30, 38, and 39 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Mura (Japanese Patent No. JP 07-302860 A) in view of Liang (U.S. Patent No. 5,350,713). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of the claims are improper because the references relied upon by the Examiner fail to teach or suggest all of the limitations of the presently claimed invention.

#### Claims 6 and 7

Each of claims 6 and 7 depend from claim 1. Claim 6 introduces the additional subject matter of forming the at least two pins of an electrically non-conductive material. Claim 7 introduces the additional subject matter of forming the at least two pins of an anti-static material.

The Examiner relies on Mura as teaching the subject matter of claim 1 and then cites Liang as disclosing the forming of nonconductive pins from a thermoplastic material.

As set forth hereinabove, Mura fails to teach or suggest all of the limitations of independent claim 1. More specifically, Mura fails to teach or suggest *providing at least two pins wherein at least one of the at least two pins includes a mechanical self-locking mechanism proximate at least one end thereof and engaging a portion of at least one of the second major surface of the semiconductor device package and a second, opposing surface of the carrier substrate with the mechanical self locking mechanism*. Applicant further submits that Liang fails to teach or suggest such subject matter. As such, claims 6 and 7 are believed to be allowable at least by virtue of their dependency from an allowable base claim.

Applicant, therefore, respectfully requests reconsideration and allowance of claims 6 and 7.

#### Claims 29 and 30

Each of claims 29 and 30 depend from claim 24. Claim 29 introduces the additional subject matter of forming the at least two pins of an electrically non-conductive material. Claim 30 introduces the additional subject matter of forming the at least two pins of an anti-static material. The Examiner relies on Mura as teaching the subject matter of claim 24 and then cites Liang as disclosing the forming of nonconductive pins from a thermoplastic material.

As set forth hereinabove, Mura fails to teach or suggest all of the limitations of independent claim 24. More specifically, Mura fails to teach or suggest *removing the pins subsequent to the alignment of each of the at least two channels with a corresponding alignment feature of the at least two alignment features*. Indeed, Mura teaches away from such subject matter in disclosing that the alignment pins are to remain between the semiconductor device package and the substrate during reflow of the solder balls thereby essentially capturing the alignment pin between the two components. As such, claims 29 and 30 are believed to be allowable at least by virtue of their dependency from an allowable base claim.

Applicant, therefore, respectfully requests reconsideration and allowance of claims 29 and 30.

**ENTRY OF AMENDMENTS**

The amendments to claims 1, 4, 6-13, 24, 27, 29-32, 36 and 43 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application.

**CONCLUSION**

Claims 1, 4, 6 through 8, 10 through 13, 24, 27, 29 through 31, 33, 35 and 36 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "Bradley B. Jensen", followed by a long horizontal line extending to the right.

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